CLAIMS

1. A multiple-mode memory comprising:

an integrated circuit substrate;

a plurality of word lines;

a plurality of bit lines crossing the word lines;

a plurality of memory cells, each memory cell coupled between a respective word line and a respective bit line, the word lines, bit lines and memory cells included in a single integrated circuit carried by the substrate;

the memory cells comprising a plurality of memory cells of a first type and a plurality of memory cells of a second type;

wherein the memory cells of the first type are programmed during manufacturing, and wherein the memory cells of the second type are programmed in the field.

2. The invention of Claim 1, wherein the memory cells of one of the first and second type have a different write time than the memory cells of the other of the first and second type.

3. The invention of Claim 1, wherein the memory cells of one of the first and second type have a different read time than the memory cells of the other of the first and second type.

4. The invention of Claim 1, wherein the memory cells of the first type store register settings, and wherein the memory cells of the second type store data.

5. The invention of Claim 1, wherein the memory cells further comprise a plurality of memory cells of a third type.

6. The invention of Claim 1, wherein the word lines are stacked in multiple levels, wherein the bit lines are stacked in multiple levels, and wherein the memory cells are stacked in multiple levels.

7. The invention of Claim 1 further comprising:

I/O circuitry carried by the substrate and coupled both with the plurality of memory cells of the first type and the plurality of memory cells of the second type via the respective word lines and bit lines.

8. A multiple-mode memory comprising:

an integrated circuit substrate;

a plurality of word lines;

a plurality of bit lines crossing the word lines;

a plurality of memory cells, each memory cell coupled between a respective word line and a respective bit line, the word lines, bit lines and memory cells included in a single integrated circuit carried by the substrate;

the memory cells comprising a plurality of memory cells of a first type and a plurality of memory cells of a second type;

wherein the memory cells of the first type store a file system structure, and wherein the memory cells of the second type store a digital media file.

9. The invention of Claim 8, wherein the memory cells of one of the first and second type have a different write time than the memory cells of the other of the first and second type.

10. The invention of Claim 8, wherein the memory cells of one of the first and second type have a different read time than the memory cells of the other of the first and second type.

11. The invention of Claim 8, wherein the memory cells further comprise a plurality of memory cells of a third type.

12. The invention of Claim 8, wherein the word lines are stacked in multiple levels, wherein the bit lines are stacked in multiple levels, and wherein the memory cells are stacked in multiple levels.

13. The invention of Claim 8 further comprising:

I/O circuitry carried by the substrate and coupled both with the plurality of memory cells of the first type and the plurality of memory cells of the second type via the respective word lines and bit lines.

14. A multiple-mode memory comprising:

an integrated circuit substrate;

a plurality of word lines;

a plurality of bit lines crossing the word lines;

a plurality of memory cells, each memory cell coupled between a respective word line and a respective bit line, the word lines, bit lines and memory cells included in a single integrated circuit carried by the substrate;

the memory cells comprising a plurality of memory cells of a first type and a plurality of memory cells of a second type;

wherein the memory cells of the first type store a different data type than the memory cells of the second type.

15. The invention of Claim 14, wherein the memory cells of one of the first and second type have a different write time than the memory cells of the other of the first and second type.

16. The invention of Claim 14, wherein the memory cells of one of the first and second type have a different read time than the memory cells of the other of the first and second type.

17. The invention of Claim 14, wherein the memory cells of the first type are assigned a different level of cache hierarchy than the memory cells of the second type.

18. The invention of Claim 14, wherein the memory cells further comprise a plurality of memory cells of a third type.

19. The invention of Claim 14, wherein the word lines are stacked in multiple levels, wherein the bit lines are stacked in multiple levels, and wherein the memory cells are stacked in multiple levels.

20. The invention of Claim 14 further comprising:

I/O circuitry carried by the substrate and coupled both with the plurality of memory cells of the first type and the plurality of memory cells of the second type via the respective word lines and bit lines.